REMARKS/ARGUMENTS

In the Office Action, the Examiner allowed claims 11 and 19 if rewritten in independent form including all of the limitations of the base claim and any intervening claims; objected to the title of the invention; rejected claims 1-4, 7, 9, 10, 12, and 13 under 35 U.S.C. 102(b) as being anticipated by *Tain* et al. (U.S. Pat. No. 6,319,752); and rejected claims 5, 6, 8, 14-18, and 20-28 under 35 U.S.C. 103(a) as being unpatentable over combinations of *Tain* et al., *Chou* et al. (U.S. Pat. No. 5,691,568), and *Kida* et al. (U.S. Pat. No. 5,877,942). The Applicants appreciate the indication of allowable subject matter. Applicants traverse the rejections for the reasons set forth below. Reconsideration is respectfully requested based on the remarks below.

Claims 1, 8, 9, 11, 17 and 19 have been amended to further clarify the subject matter regarded as the invention. Support for the amendments can be found in the specification on page 13, lines 21-35, original claims 11 and 19, and elsewhere. Claims 29-38 have been canceled without prejudice. Accordingly, claims 1-28 are now pending in this application.

ALLOWABLE SUBJECT MATTER

It is respectfully submitted that claims 11 and 19 are in condition for allowance since they have been rewritten in independent form including all of the limitations of the base claim and any intervening claims as pointed out by the Examiner.

TITLE OF THE INVENTION

It is respectfully submitted that the title has been amended as suggested by the Examiner to: "METHOD OF DESIGNING A MODULATED FLIP CHIP SUBSTRATE DESIGN".

PATENTABILITY OF CLAIMS 1-10, 12-18, 20-28

Aspects of the present invention relate to a module-based design for producing a standardized electrical interconnect design. (See page 3, lines 2-4) Claim 1 pertains to a method for designing a plurality of electrical paths in a substrate used for coupling to a die. The substrate has a plurality of layers. Claim 1 includes among other things the limitations of: "selecting modular cells for the first end section and the second end section, the modular cells being a first end modular cell and a second end modular cell" and "connecting the first end modular cell to the second end modular cell with transmission lines to form the plurality of electrical paths, the transmission lines corresponding to the intermediate section." Claim 9 recites similar limitations.

A number of benefits with respect to conventional approaches can be realized due to the standardization of a modular electrical interconnect design. For example, a consistent electrical interconnect design can be achieved between different designers despite their levels of expertise. This in turn provides a consistent electrical interconnect design between different devices within a product family. Not only will an optimized electrical interconnect design (e.g., via the applied constraints) be achievable, the electrical interconnect design will possess electrical behaviors and performances that are more predictable. Moreover, the benefit of having shorter leadtimes for generating the electrical interconnect design and reduced overall production development cycle can be realized with various aspects of the present invention. (See page 13, lines 25-35)

In contrast, the cited references do not have these advantages since they do not teach or disclose any mechanism or technique for implementing a module-based design. In particular, the cited art does not teach or suggest selecting and connecting "modular cells" as required in claims 1 and 9. *Tain* et al. discloses "creating graphic presentations of the die having the bumps and the package having pins, and placing the graphic presentation of the die into the graphic presentation of the package." (See abstract; Figs. 5 and 6) For example, *Tain* et al. discloses having a drawing of a die 300 with a pattern of bumps created using AutoCAD. (See Fig. 3) Using a design tool, such as Advanced Package Design (APD) software, a graphic presentation of a package 400 with a pin pattern is created. (See Fig. 4) The graphic presentation of die 300 is then converted from the AutoCAD format into the APD format and placed in a central portion of the graphic presentation of the package 400. (See column 3, lines 21-33; Fig. 5) However, *Tain* et al. fails to teach or suggest how the graphic presentations of die 300 and package 400 are actually created. For example, as opposed to selecting modular cells as required by claims 1 and 9, the graphic presentation of die 300 and package 400 can be created from scratch without utilizing any standardized cell construction.

Tain et al. also discloses having an autorouter "determine whether a netlist is provided." If the netlist exists, "the autorouter finds the best route from each bump to the corresponding pin as specified by the netlist." To generate the best route, "the autorouter follows a number of rules." (See column 3, lines 34-60; Fig. 6) However, as discussed above, *Tain* et al. fails to teach or suggest whether the corresponding die 300 and package 400 of the respective bumps and pins are from selected modular cells. In fact, nowhere in *Tain* et al. is there any mention of a module-based design, much less selecting and connecting "modular cells" as required in claims 1 and 9.

Kida et al. is directed to a "[c]ircuit card assembly footprint providing reworkable interconnection paths for use with a surface mount device." (See Title) *Kida* et al. merely discloses having the circuit card assembly include severable traces on a bottom surface of the assembly connecting pairs of near and far vias. The severable traces and the pairs of near and far vias allow the circuit card assembly to be selectrively re-worked to accommodate changes to the design of the surface mount device. (See Abstract) However, similar to *Tain* et al., nowhere in *Kida* et al. is there any mention of a module-based design, much less selecting and connecting "modular cells" as required in claims 1 and 9.

Chou et al. is directed to a "[w]ire bondable package design with maximum electrical performance and minimum number of layers." (See Title) *Chou* et al. merely discloses a semiconductor device package for one or more semiconductor dice having core circuits and input-output circuits using a package substrate having one pair of biplanar conductive planes and another pair of biplanar conductive planes. Power may be supplied to die core circuits through one pair of planes and to die input-output circuits through another pair of planes to decouple the core circuits from the input-output circuits and minimize noise induced false switching in either set of circuits. (See Abstract) However, again similar to *Tain* et al., nowhere in *Chou* et al. is there any mention of a module-based design, much less selecting and connecting "modular cells" as required in claims 1 and 9.

In view of the above, it is respectfully submitted that none of the cited references, either alone or in combination, teaches or suggests selecting and connecting "modular cells" as required in claims 1 and 9. That is, claims 1 and 9 are patently distinct from the cited art.

The Examiner's rejections of the dependent claims are respectfully traversed. Claims 2-8, 10, 12-18, and 20-28 each depend either directly or indirectly from independent claims 1 or 9 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1 or 9. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. ALTRP099).

Respectfully submitted,
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